[0033] Under normal operating conditions (no ESD event), the transistor and zener diode are disabled. Normal operating voltages applied to terminal **400** are insufficient to break down the zener diode. The base-emitter junction of the transistor comprising base region **430** and emitter region **370** are both coupled to ground. The base-emitter junction is not forward biased in this state, thus the transistor is off. In general, ESD protection circuit **300** does not represent a significant load to signals applied to the I/O common to terminal **400**.

[0034] The zener diode sets a voltage at which ESD protection circuit **300** is enabled. As mentioned previously, the zener diode comprises n-type region **350**, epitaxial layer **320**, and p-type region **390**. The breakdown voltage of the zener diode is a function of doping concentration and the spacing between n-type region **350** and p-type region **390**. Epitaxial layer **320** is fully depleted prior to the zener diode voltage breakdown. The breakdown voltage of the zener diode is selected based on the type of transistors or devices being protected on the integrated circuit wafer process flow. Typically, the breakdown voltage is selected to be greater than the operating voltage of the integrated circuit to prevent false triggering under normal operation.

[0035] In general, ESD protection circuit **300** acts as a voltage clamp to an ESD event. An ESD event couples a voltage impulse that can measure thousands of volts to circuitry coupled to an I/O of an integrated circuit. ESD protection circuit **300** clamps the voltage to a value that does not damage the circuitry of the integrated circuit and dissipates the energy of the pulse in a short period of time. An ESD event coupled to terminal **400** couples the voltage impulse to n-type region **350**. P-type region **390** is initially coupled to ground through base region **430**. An impact ionization current is generated as the voltage across the zener diode approaches the zener breakdown voltage of the device. The impact ionization current causes avalanche breakdown to occur in the zener diode (at the breakdown voltage of the device). The impact ionization current is coupled from p-type region **390** into base region **430**. P-type region **420** provides subsurface current paths that uniformly redistributes the impact ionization current from the surface of base region **430**. Current crowding is greatly reduced. P-type region **420** creates a redistribution of bipolar currents from the surface to flow in a more vertical manner thereby reducing power dissipation in the surface region.

[0036] The impact ionization current from the zener diode increases corresponding to the rising voltage of the ESD event. The impact ionization current in base region **430** produces a voltage that forward biases the base-emitter junction of the transistor due to the inherent resistance of the region. The enabled transistor is a high current gain device. A portion of the impact ionization current is base current to the transistor. The transistor multiplies the base current by the current gain (β) of the vertical transistor and sinks current corresponding to the ESD event. The enabled transistor clamps the voltage of the ESD event from rising and dissipates the energy the impulse.

[0037] **FIG. 5** is a graph of a transmission pulse line characteristics corresponding to ESD protection circuit **300** of **FIG. 4**. In general, transmission pulse line testing provides a pulse similar to an ESD event to the ESD protection circuit under test. The data shown is for an ESD protection circuit measuring 52.5 microns on a side. In particular, the ESD protection circuit has parameters similar to that described hereinabove. More specifically, base region **430** is approximately 2.8 microns deep. P-type region **430** is formed approximately 2 microns deep in base region **430**. The doping concentration of p-type region **430** is approximately an order of magnitude more than the doping concentration of base region **430**. The voltage and current coupled to the ESD protection circuit is monitored. Voltage is displayed on the x-axis of the graph and current on the y-axis of the graph.

[0038] An initial voltage impulse is clamped to a voltage magnitude less than 50 volts as the zener diode comprising n-type region **350**, n-type epitaxial layer **320**, and p-type region **390** breaks down providing impact ionization current to base region **430**. The impact ionization current enables the transistor by creating a voltage drop in base region **430** that forward biases the base-emitter junction. A portion of the impact ionization current is base current that is multiplied by the current gain of the transistor thereby rapidly shunting current of the ESD event through a low impedance path to ground. The voltage at terminal **400** continues to fall to approximately the breakdown voltage of the zener diode plus a base-emitter junction voltage. The test equipment measures the maximum current that can be handled by ESD protection circuit **300** before failure. The point of failure is represented by dot **510** on the curve which corresponds to a current slightly greater than 8000 milliamperes.

[0039] ESD protection circuit **300** as tested has the same area as the prior art ESD protection circuit tested in **FIG. 3**. Note that ESD protection circuit **300** has greater than twice the current handling capability of the prior art ESD protection circuit. Moreover, a difference in failure mechanism occurs that shifts from the base to the collector of the transistor (at 8000 milliamperes the failure occurs at the collector of the transistor). The increase in maximum current that can be handled by ESD protection circuit **300** directly translates to better protection against higher energy ESD events. A further benefit of ESD protection circuit **300** is that the cell size can be reduced while providing the same benefit of the prior art ESD protection circuit thereby reducing the die size of the integrated circuit. ESD protection circuit **300** is easily implemented in many common wafer process flows without the need of extra processing steps. Furthermore, the design is robust and scalable from a processing perspective thereby allowing it to be used in future generation process flows.

[0040] **FIG. 6** is a top view of an ESD protection circuit **300** in accordance with the present invention. The top view is representative of the ring shapes described in **FIG. 4**. P-type region **340** is formed in a ring shape that isolates ESD protection circuit **300** from other devices (not shown) of the integrated circuit. The active area in which ESD protection circuit **300** is formed is interior to p-type region **340**. P-type region **340** is coupled to ground.

[0041] N-type region **350** is formed in a ring shape in the active area and contacts the buried layer (not shown) underlying the base region of the transistor. P-type region **390** is formed in a ring shape interior to the ring shape of n-type region **350**. The zener diode comprises p-type region **390**, the epitaxial layer (not shown), and n-type region **350**. P-type region **390** couples to the base region (not shown).